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1609 7590 12/19/2007 ROYLANCE, ABRAMS, BERDO & GOODMAN, L.L.P. 1300 19TH STREET, N.W. SUITE 600 WASHINGTON,, DC 20036				
			EXAMINER SPITTLE, MATTHEW D	
			ART UNIT 2111	PAPER NUMBER
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/759,232

Applicant(s)

CHUNG ET AL.

Examiner

Matthew D. Spittle

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 11 October 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-14, 19-24, 26 and 38-42 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14, 19-24, 26 and 38-42 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 May 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 10/10/2007.
- ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- ☐ Notice of Informal Patent Application
- ☐ Other: \_\_\_\_\_.

### DETAILED ACTION

Claims 1 – 14, 19 – 24, 26, and 38 – 42 have been examined.

#### ***Claim Rejections - 35 USC § 112***

5       The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

10       Claim 33 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

15       Claim 33 recites, "...a controller unit..." Examiner is unable to find support in Applicant's disclosure for such a component, and request that Applicant provide specific evidence from the specification for this device.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

20       The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

      Claims 1, 2, 5, 7, 8, 9, and 12 rejected under 35 U.S.C. 112, second paragraph,  
25       as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claims 1, 2, 5, 7, 8, 9 and 12, Examiner is unclear as to what data the "bit strings" refers to.

Claim 1 recites, "...storing the bit strings configuring the read data in a DMA control register..." Examiner interprets those bit strings as the bits that are stored in the DMA control register to configure the read data.

Claim 12, as an example, recites, "...rearranges positions of less and more significant bit strings, and writes the read data to the second storage medium according to a result of the rearrangement." In this part of claim 12, the meaning of bit strings appears to refer to the manipulated read data. For this reason, Examiner finds the meaning of "the bit strings" in claims 1, 2, 5, 6, 8, 9 and 12 to be ambiguous since the claim does not distinguish between the two apparent types of bit strings that are used.

Claims 36, 38, 40 and 42 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims recite either setting/resetting the DMA activation bit when the amount of data is large or small. It is not clear what is meant since both "large" and "small" are relevant terms, and meaningless without defining a range which clearly specifies the size of the data. Therefore, the claims are held to be indefinite.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the

Art Unit: 2111

subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1 – 4 , 35 and 37 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Tokumaru in view of Staplin et al. and what is old and well known in the art as evidenced by Archer et al. (U.S. 5,517,626), Bailey et al. (U.S. 5,548,587), DuLac (U.S. 4,965,801), Johnson et al. (U.S. 4,878,166), and Burrus et al. (U.S. 4,716,523).

With regard to claim 1, Tokumaru teaches a method for reading and storing data by means of a direct memory access (DMA) medium (Figure 4), comprising the steps of:

In the DMA medium (interpreted as a DMA controller), deciding a shift direction and a predetermined number of bits to be shifted in advance (column 3, line 64 – column 4, line 3; column 4, lines 18 – 22) when a request is made so that data read from a first storage medium (where a first storage medium may be interpreted as a first memory; column 3, lines 23 – 29) can be processed;

Shifting the bit strings by the predetermined number of bits in the decided shift  
80 direction, and transferring the shifted bit strings to a second storage medium (where a  
second storage medium may be interpreted as a destination memory; column 3, lines  
23 – 29; column 2, lines 45 – 56).

Tokumaru fails to teach sequentially storing bit strings configuring the read data  
in a DMA control register.

85 Staplin et al. teach sequentially storing bit strings configuring the read data  
(specifically, the shift direction and number of shifts) in a register (interpreted as an F-  
register; Figure 3, item 51; column 9, lines 18 – 24; Table 1).

It would have been obvious to one of ordinary skill in this art at the time of  
invention by applicant to store the shift configuring data as taught by Tokumaru into a  
90 register as taught by Staplin et al. This would have been obvious in order to store the  
configuration values, thereby making it unnecessary to re-compute them in the case  
where an identical operation is performed twice in a row, thus, making the DMA  
operation more efficient.

Staplin et al. and Tokumaru both fail to teach determining whether a DMA  
95 activation status is set to active for the DMA to perform data transmission, and reading  
data if the DMA activation status is set to active.

Examiner takes Official Notice that DMA activation status stored in a control  
register is old and well known in the art. This is evidenced by Burrus et al. (col. 35, lines  
23 – 25, 28 – 30), Johnson et al. (col. 32, lines 24 – 32), DuLac (col. 7, line 66 – col. 8,  
100 line 5), Bailey et al. (Fig. 8), and Archer et al. (col. 66, line 60 – col. 7, line 13).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate a register containing a DMA activation status for the purpose of enabling and disabling DMA transfers. This would have been obvious since to do so is routine in the art.

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With regard to claim 2, Staplin et al. teach the additional limitation wherein each of the bit strings configuring the read data is configured by one of an 8-bit string, a 16-bit string, or a 32-bit string (column 12, lines 12 – 13).

110

With regard to claim 3, Staplin et al. teach the additional limitation wherein the number of bits to be shifted has a value from 0 to 7 (column 9, lines 50 – 55; Staplin et al. teach that 4 bits (bits 12 – 15) are used when bit 8 equals a binary 0 to determine the number of positions to be shifted. 4 bits would provide a range from 0 to 15).

115

With regard to claim 4, Tokumaru teaches the additional limitation wherein the step of deciding the shift direction and the number of bits to be shifted depends upon bit values set by the DMA medium (Examiner interprets the shifting signals, which determine the shift direction and number of bits (column 3, line 64 – column 4, line 3; column 4, lines 18 – 22) as being part of the DMA medium, and therefore the reference

120

meets this limitation).

Regarding claim 35, Bailey et al. teach the additional limitation wherein the DMA activation status is set to active when a DMA activation bit is set to 1 (Fig. 8, bit 4, see description).

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Regarding claim 37, Bailey et al. teach the additional limitation wherein the DMA activation status is not set to active when a DMA activation bit is set to 0 (Fig. 8, bit 4, see description).

130

Regarding claims 36 and 38, the terms "large" and "small" are given their broadest reasonable interpretation, and thus it is inherent in Archer et al., Bailey et al., DuLac, Johnson et al., and Burrus et al. for the DMA activation bit to be set to 1 or 0 when the data is large or small, respectively, since all of the said references teach transmitting data both through DMA transfer (having the bit enabled) or not (having the bit disabled).

135

\* \* \*

Examiner assumes that the applicant meant to recite classifying the read data, instead of classifying the bit strings configuring the read data in the following:

140

Claims 5 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al., and further in view of Beukema et al.



With regard to claim 5, Tokumaru and Staplin et al. teach writing the bit strings configuring the read data to the second storage medium, but fail to teach classifying the  
145 bit strings configuring the read data into more significant bit strings and less significant bit strings; and rearranging positions of less and more significant bit strings.

Beukema et al. teach classifying bit strings into more significant bit strings and less significant bit strings and rearranging positions of less and more significant bit strings (Figure 6B, 7B, 8; where classifying bit strings and rearranging positions may be  
150 interpreted as reflection; column 9, lines 41 – 60; column 16, lines 60 – 67).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the method of Beukema into the method of Tokumaru and Staplin et al. This would have been obvious in order to provide DMA transfers on “mixed endian computing systems” in order to promote better performance  
155 when converting between the two types of data organization (column 2, lines 38 – 43; column 3, lines 51 – 56).

With regard to claim 6, Beukema et al. teach the additional limitation of wherein the bit strings configuring the read data is configured in the form of 32 bits at the step of  
160 rearranging the positions of the less and more significant bit strings (Figure 4C; column 5, lines 52).

With regard to claim 7, Beukema et al. teach the additional limitation of wherein the step of rearranging the positions of the less and more significant bit strings depends

165 upon bit values set by the DMA medium (where a bit value may be interpreted as a  
"reflection bit" (RB); column 9, lines 41 – 58).

\* \* \*

170 Claims 8 – 11, 39 and 41 are rejected under 35 U.S.C. 103(a) as being  
unpatentable over Tokumaru in view of Staplin et al. and what is old and well known in  
the art as evidenced by Archer et al. (U.S. 5,517,626), Bailey et al. (U.S. 5,548,587),  
DuLac (U.S. 4,965,801), Johnson et al. (U.S. 4,878,166), and Burrus et al. (U.S.  
4,716,523).

175 With regard to claim 8, Tokumaru teaches an apparatus for reading and storing  
data by means of a director memory access (DMA) medium (Figure 4), comprising:

A first storage medium for storing data read in a source address (where a first  
storage medium may be interpreted as a first memory; column 3, lines 23 – 29) ;

The DMA medium for decoding a shift direction and a predetermined number of  
180 bits to be shifted in advance when a request is made so that the read data can be  
processed, sequentially storing bit strings configuring the read data, shifting the bit  
strings by the predetermined number of bits in the decided shift direction, and  
transferring the shifted bit strings (column 3, line 64 – column 4, line 3; column 4, lines  
18 – 22);

185           A second storage medium for storing data transferred from the DMA medium  
(where a second storage medium may be interpreted as a destination memory; column  
3, lines 23 – 29; column 2, lines 45 – 56).

Tokumaru fails to teach sequentially storing bit strings configuring the read data  
in a DMA control register.

190           Staplin et al. teach sequentially storing bit strings configuring the read data  
(specifically, the shift direction and number of shifts) in a register (interpreted as an F-  
register; Figure 3, item 51; column 9, lines 18 – 24; Table 1).

It would have been obvious to one of ordinary skill in this art at the time of  
invention by applicant to store the shift configuring data as taught by Tokumaru into a  
195 register as taught by Staplin et al. This would have been obvious in order to store the  
configuration values, thereby making it unnecessary to re-compute them in the case  
where an identical operation is performed twice in a row, thus, making the DMA  
operation more efficient.

Staplin et al. and Tokumaru both fail to teach determining whether a DMA  
200 activation status is set to active for the DMA to perform data transmission, and reading  
data if the DMA activation status is set to active.

Examiner takes Official Notice that DMA activation status stored in a control  
register is old and well known in the art. This is evidenced by Burrus et al. (col. 35, lines  
23 – 25, 28 – 30), Johnson et al. (col. 32, lines 24 – 32), DuLac (col. 7, line 66 – col. 8,  
205 line 5), Bailey et al. (Fig. 8), and Archer et al. (col. 66, line 60 – col. 7, line 13).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate a register containing a DMA activation status for the purpose of enabling and disabling DMA transfers. This would have been obvious since to do so is routine in the art.

210

With regard to claim 9, Staplin et al. teach the additional limitation wherein the DMA medium reads each of the bit strings configuring the data with one of an 8-bit string, a 16-bit string, or a 32-bit string (column 12, lines 12 – 13).

215

With regard to claim 10, Staplin et al. teach the additional limitation wherein the DMA medium carries out the shift operation according to the number of bits to be shifted that has a value from 0 to 7 (column 9, lines 50 – 55; Staplin et al. teach that 4 bits (bits 12 – 15) are used when bit 8 equals a binary 0 to determine the number of positions to be shifted. 4 bits would provide a range from 0 to 15).

220

With regard to claim 11, Tokumaru teaches the additional limitation wherein the DMA medium decides the shift direction and the number of bits to be shifted depends upon bit values (Examiner interprets the shifting signals, which determine the shift direction and number of bits (column 3, line 64 – column 4, line 3; column 4, lines 18 – 22) as being part of the DMA medium, and therefore the reference meets this limitation).

225

Regarding claim 39, Bailey et al. teach the additional limitation wherein the DMA activation status is set to active when a DMA activation bit is set to 1 (Fig. 8, bit 4, see description).

Regarding claim 41, Bailey et al. teach the additional limitation wherein the DMA activation status is not set to active when a DMA activation bit is set to 0 (Fig. 8, bit 4, see description).

Regarding claims 40 and 42, the terms "large" and "small" are given their broadest reasonable interpretation, and thus it is inherent in Archer et al., Bailey et al., DuLac, Johnson et al., and Burrus et al. for the DMA activation bit to be set to 1 or 0 when the data is large or small, respectively, since all of the said references teach transmitting data both through DMA transfer (having the bit enabled) or not (having the bit disabled).

\* \* \*

Examiner assumes that the applicant meant to recite classifying the read data, instead of classifying the bit strings configuring the read data in the following:

Claim 12 – 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al., Beukema et al. and what is old and well known in the

Art Unit: 2111

art as evidenced by Archer et al. (U.S. 5,517,626), Bailey et al. (U.S. 5,548,587), DuLac  
250 (U.S. 4,965,801), Johnson et al. (U.S. 4,878,166), and Burrus et al. (U.S. 4,716,523).

With regard to claim 12, Tokumaru and Staplin et al. teach writing the bit strings  
configuring the read data to the second storage medium, but fail to teach the DMA  
medium classifying the bit strings configuring the read data into more significant bit  
strings and less significant bit strings; and rearranging positions of less and more  
255 significant bit strings.

Beukema et al. teach the DMA medium classifying bit strings into more  
significant bit strings and less significant bit strings and rearranging positions of less and  
more significant bit strings (Figure 6B, 7B, 8; where classifying bit strings and  
rearranging positions may be interpreted as reflection; column 9, lines 41 – 60; column  
260 16, lines 60 – 67).

It would have been obvious to one of ordinary skill in this art at the time of  
invention by applicant to incorporate the method of Beukema into the method of  
Tokumaru and Staplin et al. This would have been obvious in order to provide DMA  
transfers on “mixed endian computing systems” in order to promote better performance  
265 when converting between the two types of data organization (column 2, lines 38 – 43;  
column 3, lines 51 – 56).

With regard to claim 13, Beukema et al. teach the additional limitation of wherein  
the DMA medium rearranges the positions of the less and more significant bit strings

270 when the bit strings configuring the read data is configured in the form of 32 bits (Figure 4C; column 5, lines 52).

With regard to claim 14, Beukema et al. teach the additional limitation of wherein the DMA medium rearranges the positions of the less and more significant bit strings  
275 depends upon bit values (where a bit value may be interpreted as a "reflection bit" (RB); column 9, lines 41 – 58).

\* \* \*

280 Claims 19, 20, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al., Black (OSI – A Model for Computer Communications Standards), and what is old and well known in the art as evidenced by Archer et al. (U.S. 5,517,626), Bailey et al. (U.S. 5,548,587), DuLac (U.S. 4,965,801), Johnson et al. (U.S. 4,878,166), and Burrus et al. (U.S. 4,716,523

285 Regarding claim 19, Tokumaru and Staplin et al. fail to explicitly teach the limitations including first and second layers, however, Examiner notes that both Tokumaru and Staplin et al. are geared toward improving communication between computer systems and components.

Black provides a set of standards that allow for compatible communications  
290 between varying types of computer systems and hardware, including:

At a second layer, receiving at least one first layer data packet from a first layer and storing said at least one first layer data packet in the first storage medium which corresponds to the second layer by shifting said at least one first layer data packet by as many bits as indicated by a second layer header (p. 7 – 9; p. 31, Fig. 1-14);

295 Adding the second layer header in front of said at least one first layer data packet to make a second layer data packet (as shown on p. 7, Fig. 1-2);

Transferring at least one second layer data packet to a third layer (p. 9, Fig. 1-3),

Wherein said second layer header includes control information for said second layer data packet (p. 33, par. 1 – 3).

300 Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the OSI model as taught by Black into the computer communication systems of Tokuramu and Staplin et al. for the purpose of providing a standardized means of communication between multiple systems. This would have been obvious in order to make the systems compatible with one another,  
305 thereby offering more flexibility to the user in terms of software and hardware selection.

Regarding claim 20, Black teaches the additional limitation comprising:

At said third layer, receiving said at least one second layer data packet and storing said at least one second layer data packet in the second storage medium which  
310 corresponds to the third layer (p. 9, Fig. 1-3);

Adding cyclic redundancy checking (CRC) at the rear of said at least one second layer data packet to make a third layer data packet (p. 32 – 33, 114 – 115, 285).



Regarding claim 24, Tokumaru teaches the additional limitation wherein the  
315 transfer between the layers is performed by direct memory access (DMA) (ABSTRACT).

Regarding claim 26, Black teaches the additional limitation wherein the shift  
direction and size of bits to be shifted is decided according to information in a header (p.  
31, Fig. 1-14 shows how the packet bits are shifted when the header is added to the  
320 packet as it travels between layers. Thus Black inherently teaches the limitation of  
shifting and shift direction.).

\* \* \*

325 Claims 21 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over  
Tokumaru in view of Staplin et al. and Black (OSI – A Model for Computer  
Communications Standards), what is old and well known in the art as evidenced by  
Archer et al. (U.S. 5,517,626), Bailey et al. (U.S. 5,548,587), DuLac (U.S. 4,965,801),  
Johnson et al. (U.S. 4,878,166), and Burrus et al. (U.S. 4,716,523), and what is old and  
330 well known in this art as evidenced by Lundsjo et al. (U.S. 6,473,442), Chuah et al.  
(U.S. 6,400,695), Hamalainen et al. (U.S. 6,359,904) and Yi et al. (U.S. 7,054,270).

Regarding claims 21 – 23, Black teaches wherein the third layer comprises a  
physical (PHY) layer (p. 9, Fig 1-3), but fails to explicitly teach wherein the first layer is a

Art Unit: 2111

radio link control (RLC) layer and the second layer is a medium access control (MAC)

335 layer.

Examiner takes Official Notice that a protocol stack of this type is old and well known in this art. This is evidenced by Lundsjo et al. (Fig. 2), Chuah et al. (Fig. 2), Hamalainen et al. (Fig. 2a), and Yi et al. (Fig. 1).

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\* \* \*

Claims 28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tokumaru in view of Staplin et al., Black (OSI – A Model for Computer Communications Standards) and what is old and well known in the art as evidenced by Archer et al. (U.S. 5,517,626), Bailey et al. (U.S. 5,548,587), DuLac (U.S. 4,965,801), Johnson et al. (U.S. 4,878,166), and Burrus et al. (U.S. 4,716,523).

345

Regarding claim 28, Tokumaru and Staplin et al. fail to explicitly teach the limitations including first and second layers, however, Examiner notes that both Tokumaru and Staplin et al. are geared toward improving communication between computer systems and components.

350

Black provides a set of standards that allow for compatible communications between varying types of computer systems and hardware, including:

Wherein a data packet is generated in a mobile communication system (interpreted as a computer) and data is shifted by means of a protocol layer (as shown on p. 31, Fig. 1-14) , and the DMA operates to transfer at least one first layer data

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Art Unit: 2111

packet from a first layer to a second layer, said second layer to receive said at least one first layer data packet from a first layer, to store said at least one first layer data packet in the first storage medium which corresponds to the second layer by shifting said at least one first layer data packet by as many bits as indicated by a second layer header, to add the second layer header in front of said at least one first layer data packet to make a second layer data packet and to transfer at least one second layer data packet to a third layer, said second layer header comprising control information for said second layer data packet (p. 7 – 9; Fig 1-2; Fig. 1-3; p. 33, par. 1 – 3).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by Applicant to incorporate the OSI model as taught by Black into the computer communication systems of Tokuarmu and Staplin et al. for the purpose of providing a standardized means of communication between multiple systems. This would have been obvious in order to make the systems compatible with one another, thereby offering more flexibility to the user in terms of software and hardware selection.

Regarding claim 29, Black teaches the additional limitation comprising:

At said third layer, receiving said at least one second layer data packet and storing said at least one second layer data packet in the second storage medium which corresponds to the third layer (p. 9, Fig. 1-3);

Adding cyclic redundancy checking (CRC) at the rear of said at least one second layer data packet to make a third layer data packet (p. 32 – 33, 114 – 115, 285).

\* \* \*

380           Claims 30 – 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over  
Tokumaru in view of Staplin et al. and Black (OSI – A Model for Computer  
Communications Standards), what is old and well known in this art as evidenced by  
Lundsjo et al. (U.S. 6,473,442), Chuah et al. (U.S. 6,400,695), Hamalainen et al. (U.S.  
6,359,904) and Yi et al. (U.S. 7,054,270), and what is old and well known in the art as  
385           evidenced by Archer et al. (U.S. 5,517,626), Bailey et al. (U.S. 5,548,587), DuLac (U.S.  
4,965,801), Johnson et al. (U.S. 4,878,166), and Burrus et al. (U.S. 4,716,523).

              Regarding claims 30 – 32, Black teaches wherein the third layer comprises a  
physical (PHY) layer (p. 9, Fig 1-3), but fails to explicitly teach wherein the first layer is a  
radio link control (RLC) layer and the second layer is a medium access control (MAC)  
390           layer.

              Examiner takes Official Notice that a protocol stack of this type is old and well  
known in this art. This is evidenced by Lundsjo et al. (Fig. 2), Chuah et al. (Fig. 2),  
Hamalainen et al. (Fig. 2a), and Yi et al. (Fig. 1).

395           Claim 34 recites limitations substantially similar as in claims 1 and 19 – 27, and is  
therefore rejected under the same grounds.

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***Response to Arguments***

Applicant's arguments with respect to claims 1 – 34 have been considered but are moot in view of the new ground(s) of rejection.

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Examiner takes Official Notice that DMA activation status stored in a control register is old and well known in the art. This is evidenced by Burrus et al. (col. 35, lines 23 – 25, 28 – 30), Johnson et al. (col. 32, lines 24 – 32), DuLac (col. 7, line 66 – col. 8, line 5), Bailey et al. (Fig. 8), and Archer et al. (col. 66, line 60 – col. 7, line 13).

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Regarding Applicant's argument that Black fails to teach the limitations of claim 19, Examiner notes that Applicant has stated that "Black does not disclose the features relating to a first and second layer as described in the claim, and fails to make up for Tokumaru and Staplin's deficiencies." This amounts to a mere allegation of patentability, and thus fails to comply with 37 CFR 1.111(b). The arguments do not specifically point out how the language of the claims patentably distinguishes them from the references.

415

Regarding Applicant's traversal of the Official Notice for showing a "protocol stack," Examiner has cited references to Lundsjo et al. (Fig. 2), Chuah et al. (Fig. 2), Hamalainen et al. (Fig. 2a), and Yi et al. (Fig. 1). All of these references show the well known protocol stack in the figures.

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Regarding Applicant's arguments pertaining to claims 5 – 7 and 12 – 14, see the above 112 2<sup>nd</sup> paragraph rejection.

Therefore, the Examiner cannot allow the claims.

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### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

430

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

435

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.


440

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

445 Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should  
450 you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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MDS

  
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